

## A 2.4GHz Low Noise Amplifier (LNA)

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## Introduction

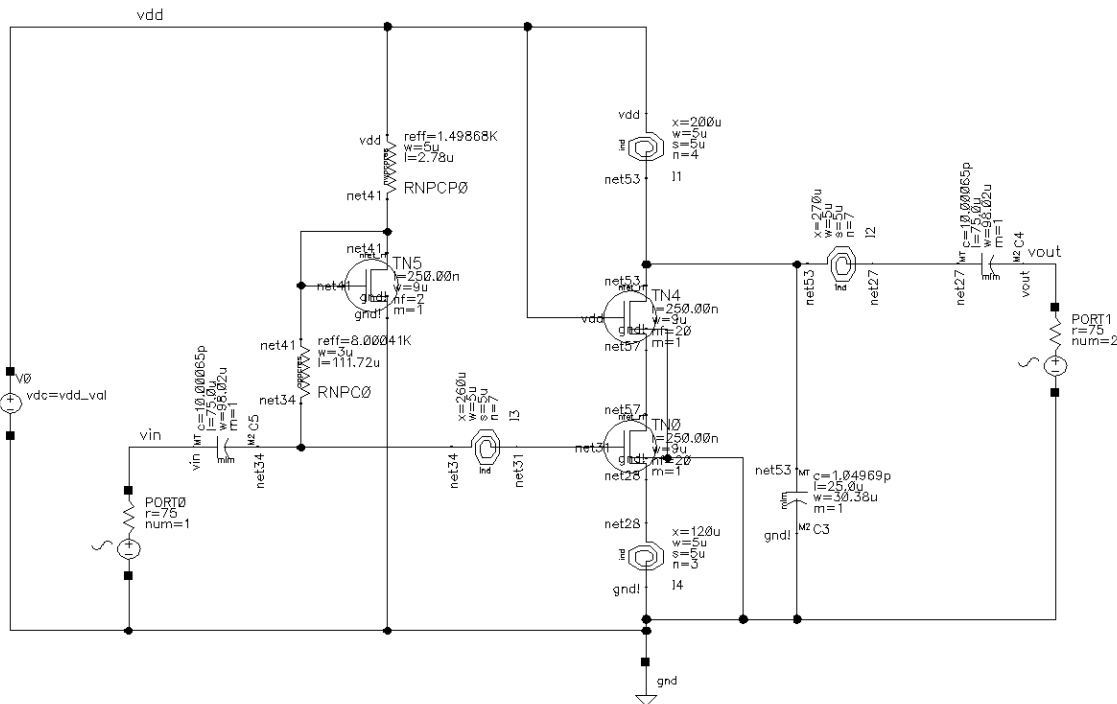
This paper describes a LNA designed in the IBM 0.25um RF CMOS process. The LNA has a single tuned frequency of 2.4GHz. The LNA is a simple class A amplifier. The following is a summary of the specification requirements and simulation results:

Parameter	Specification	Simulation Result	Units
$S_{11}$ input return loss	< -20	-22.7	dB
$S_{22}$ output return loss	< -20	-20.54	dB
$S_{21}$ power gain	> 15	16.5	dB
Noise Figure	< 1.8	2.09	dB
IP3	> -10	-0.26	dBm
1 dB compression point	None	-17	dBm
Power consumption	None	28.75	mW

**Table 1:** Compliance Matrix.

## LNA Topology

The LNA is based on the architecture described in [1]. The following is a schematic of the LNA:



**Figure 1:** LNA Schematic

The LNA is a simple class A amplifier, with some small enhancements. Cascode device TN4 is inserted to reduce the Miller capacitance on the gate of the amplifier device TN0. TN5 is a simple diode connected device which sets the bias current of the amplifier TN0. Starting at the left, C5 is a DC blocking capacitor used to couple the AC signal to the amplifier. RNPCC0 is an AC current blocking device to isolate the amplifier from the bias circuit. RNPCC0 sets the bias current for the diode connected device. This current is then mirrored to TN0 and multiplied up by a factor of approximately 10. Mirroring will not be so accurate due to the short device lengths that are necessary to minimize gate area for the sake of noise. I3 is the input inductor which is necessary to tune the input resonant frequency. The source inductor, I4, is sized to impedance to match the input of the amplifier to the output impedance of the signal source. This

inductor also behaves as a source degeneration device and as such it linearizes the gain, but also degrades the gain.

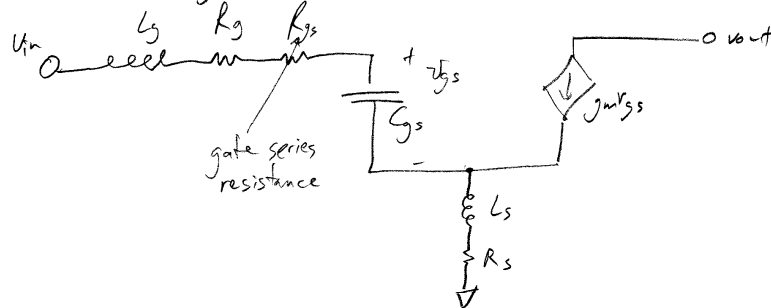
Inductor II behaves as a load to the class A amp. The reason inductors are used instead of resistors in the LNA design is two-fold. The first reason is to keep the noise down, resistors are very noisy and their noise is directly proportional to their size. The second reason is to tune the LNA to a specific frequency so the amplifier can reject some out of band signals.

### Design Equations

The following are the design equations derived from the small signal model of the circuit in Figure 1.

1.

LNA small signal model



$$V_{in} = I_{in} (sL_g + R_g + R_{gs} + \frac{1}{sC_{gs}}) + V_s$$

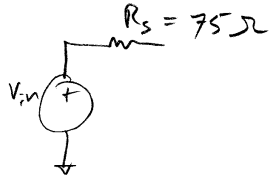
$$\begin{aligned} V_{in} &= I_{in} (sL_g + R_g + R_{gs} + \frac{1}{sC_{gs}}) + (I_{in} + g_m V_{gs})(sL_s + R_s) \\ &= I_{in} (sL_g + R_g + R_{gs} + \frac{1}{sC_{gs}}) + (I_{in} + g_m I_{in} \frac{1}{sC_{gs}})(sL_s + R_s) \end{aligned}$$

$$\begin{aligned} \frac{V_{in}}{I_{in}} &= sL_g + R_g + R_s + \frac{1}{sC_{gs}} + (1 + \frac{g_m}{sC_{gs}})(sL_s + R_s) \\ &= sL_g + R_g + R_{gs} + \frac{1}{sC_{gs}} + sL_s + R_s + \frac{g_m L_s}{C_{gs}} + \frac{g_m R_s}{sC_{gs}} \\ &= s(L_g + L_s) + \frac{1}{sC_{gs}} (1 + g_m R_s) + R_g + R_{gs} + R_s + \frac{g_m L_s}{C_{gs}} \end{aligned}$$

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + R_g + R_{gs} + R_s + \frac{g_m L_s}{C_{gs}}$$

# LNA Design

$$F = 2.4 \text{ GHz} = 15.1 \text{ rad/s}$$



$$S_{11} < -20 \text{ dB}$$

$$S_{22} < -20 \text{ dB}$$

$$S_{21} > 15 \text{ dB} \leftarrow \text{power gain}$$

$$\text{noise figure} < 1.8 \text{ dB}$$

$$I_{\text{BIAS}} = 10 \text{ mA}$$

$$C_{\text{ox}} = 5 \text{ mF/cm}^2$$

$$C_{\text{ox}} = \frac{K_{\text{ox}} \epsilon_0}{t_{\text{ox}}}$$

$$t_{\text{ox}} = 6.2 \text{ nm}$$

$$K_{\text{ox}} \leq 3.9$$

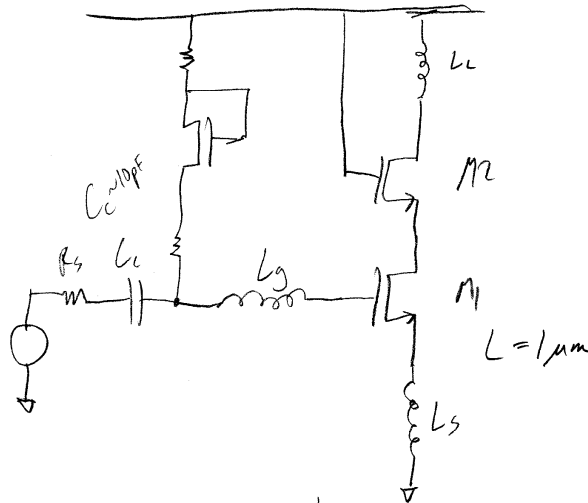
$$\epsilon_0 = 8.854 \times 10^{-14} \frac{\text{F}}{\text{cm}}$$

$$5.57 \text{ mF/cm}^2$$

$$.0056 \text{ F/cm}^2$$

$$5.6 \times 10^{-3} \text{ F/m}^2$$

$$K' = 190 \text{ mV}^2$$



$$W = \frac{1}{3 \omega \cdot L \cdot C_{\text{ox}} \cdot R_s} = 53 \mu\text{m}$$

$$50 \approx \frac{g_m L_s}{C_{gs}}$$

$$C_{gs} = \frac{2}{3} \omega \cdot L \cdot C_{\text{ox}} = 0.2 \text{ pF}$$

$$L_s = \frac{50 \cdot C_{gs}}{g_m} = 0.7 \text{ nH}$$

$$g_m = \sqrt{2 K' \frac{W}{L} I} \quad I = 10 \text{ mA}$$

$$g_m = 14.2 \text{ mS}$$

Find  $L_g$ :

$$0 = s(L_g + L_s) + \frac{1}{sC_{gs}}$$

$$0 = s^2(L_g + L_s) + \frac{1}{C_{gs}}$$

$$\omega^2 = \frac{1}{C_{gs}(L_g + L_s)} \Rightarrow \frac{1}{C_{gs} \cdot \omega^2} = L_g + L_s$$

$$L_g = \frac{1}{C_{gs} \cdot \omega^2} + L_s$$

$$= 22.6 \text{ nH}$$

$$A = g_{m1} Q_{is} z_e$$

$$Q_{is} = \frac{1}{\omega \cdot C_{gs} \cdot R_s} = 4.4$$

desired gain  $> 15 \text{ dB}$

so pick a little higher, say  $18 \text{ dB} = 8x$

$$z_e = \frac{8}{g_{m1} Q_{is}} = 128 = sL$$

$$L_L = 8.5 \text{ nH}$$

---

from sims:

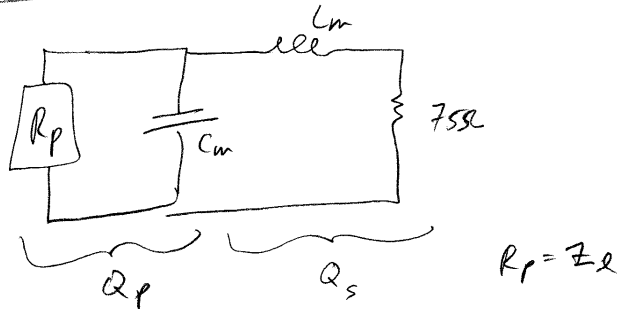
$$R_{bias} = 960$$

$$L_m = 8 \text{ nH}$$

$$L_g = 13 \text{ nH}$$

$$C_{res} = 1 \text{ pF}$$

## Impedance transformation calculation



$$Q_p = Q_s = \sqrt{\frac{R_p}{75} - 1} = 0.84$$

$$Q_p = \frac{R_p}{X_{C_m}} = 0.84 \Rightarrow \underline{C_m = 435 \text{ fF}}$$

$$Q_s = \frac{\omega L_m}{75} \Rightarrow \underline{L_m = 4.2 \text{ nF}}$$

These calculated values are a good starting point. They are not useful for much more than that because this is a very non-linear system with complex interdependencies. Through simulation almost all of these values were tweak to provide optimum performance.

## Simulation Results

### DC Solution

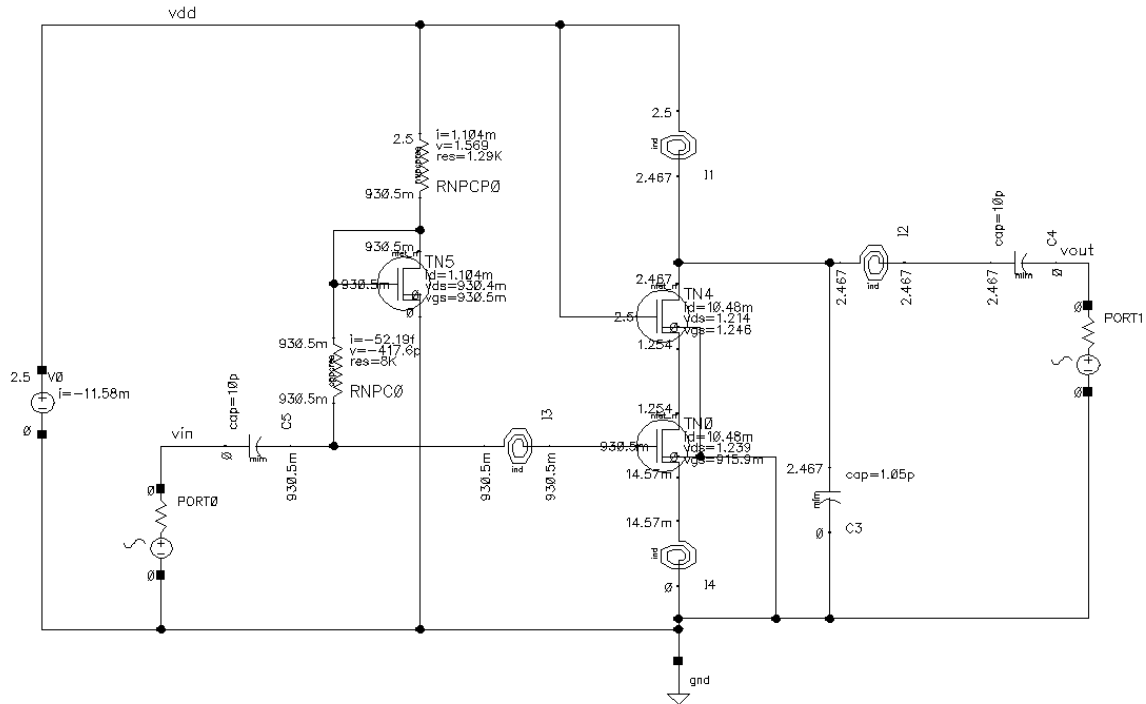
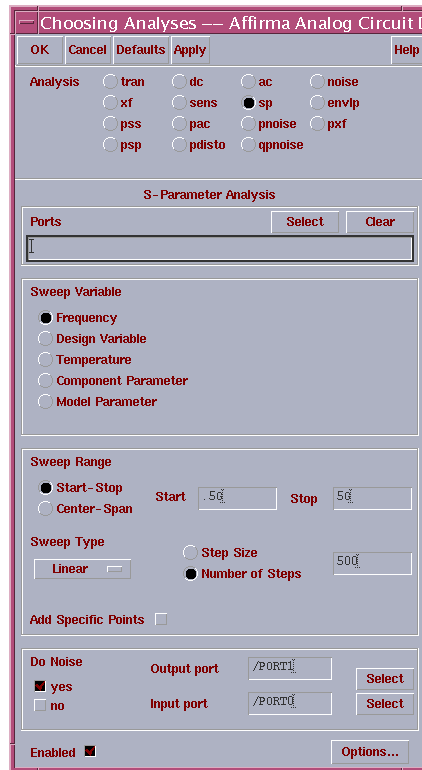


Figure 2: DC simulation results

During DC simulations all the inductors are shorts, therefore we basically have a glorified current mirror. We have 1.1mA through the bias device and 10.48mA through the amplifier device. This is slightly under the current mirror target ratio of 10. Also, with the device sizes chosen and the current, we should be well within the saturation region.

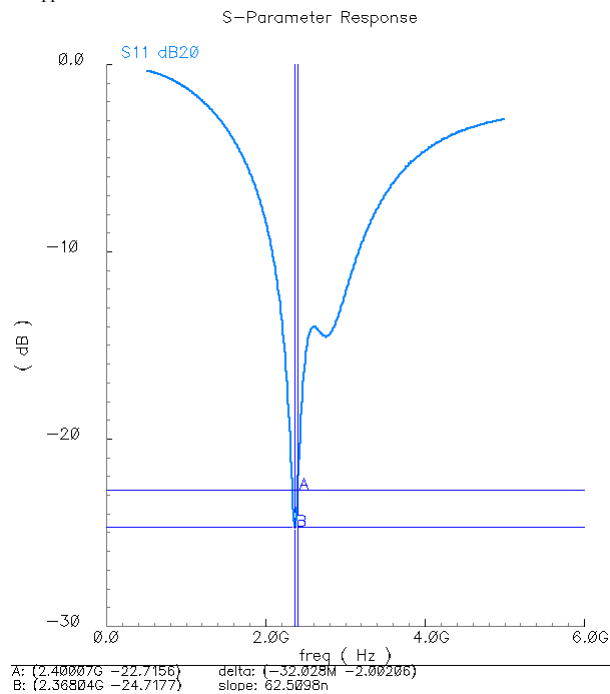
### $S_{11}$ Input Return Loss

All S-parameters were simulated using the following simulator setup:



**Figure 3:** S-parameter simulation setup.

Here are the results for the  $S_{11}$  simulation:

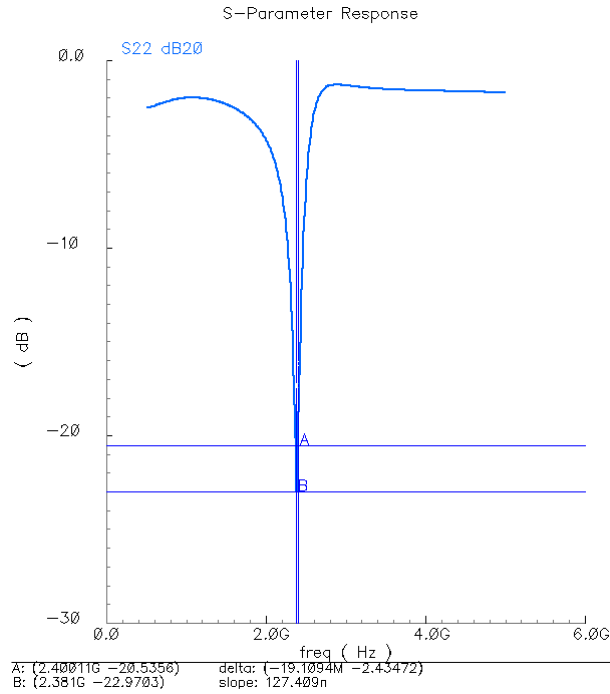


**Figure 4:**  $S_{11}$  simulation results.

Cursor A marks the Input return loss at the fundamental frequency (-22.7dBm) and cursor B marks the minimum (-24.7dBm). The magnitude of this response can be varied by tweaking the source inductor and the fundamental frequency can be modified by tweaking the gate inductor.

## S<sub>22</sub> Output Return Loss

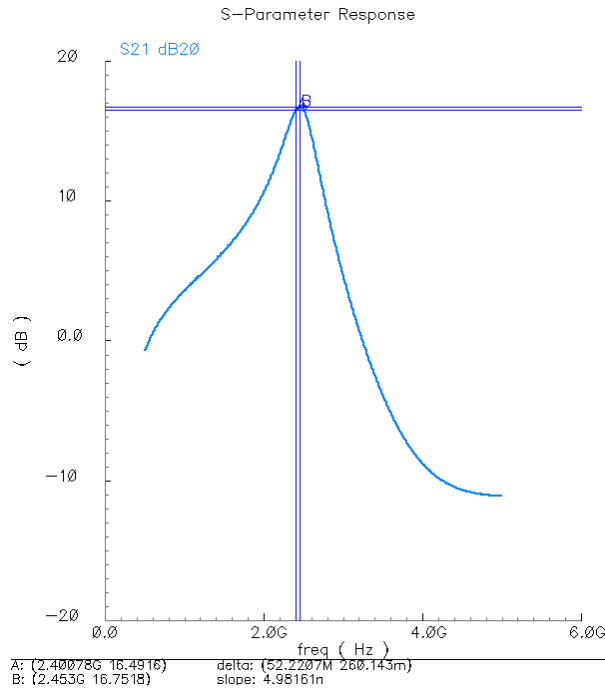
Output return loss is a measure of the output power transfer lost due to a mismatch between the output impedance of the LNA and the load. Inductor I2 and capacitor C3 (see figure 1) form the matching network to match the impedance of the output of the LNA to the load. Inductor I2 can be tweaked to minimize the loss.



**Figure 5:** S<sub>22</sub> simulation results.

Cursor A marks the output return loss at the fundamental frequency (-20.5 dBm) and cursor B marks the minimum (-23 dBm).

## S<sub>21</sub> Power Gain



**Figure 6: Power Gain.**

Cursor A marks the gain at the fundamental frequency (16.5 dB) and cursor B marks the maximum (16.75). The gain is tuned very well, the gate inductor sets the resonant frequency.

## Noise Figure

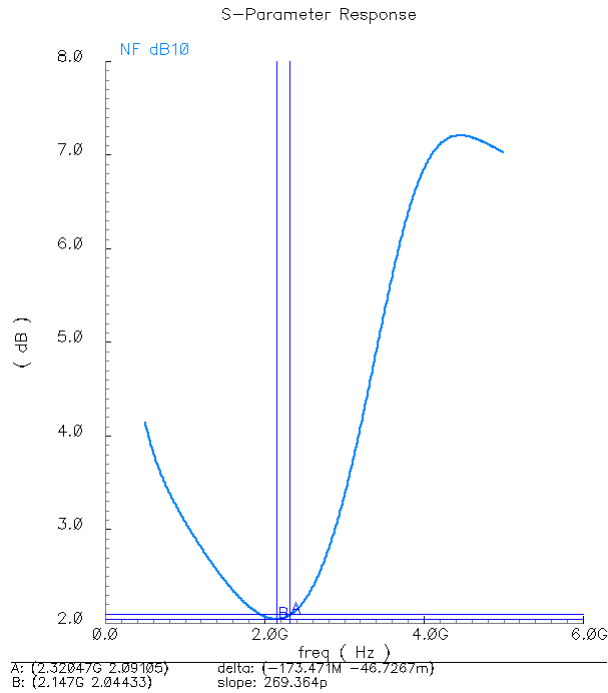
The noise figure is derived from the Noise Factor as below:

$$NF(dB) = 10 \cdot \log(F)$$

where F is the noise factor. The noise factor is defined as the ratio of the carrier power of the input to the thermal noise of the input to the carrier power at the output to the thermal noise at the output, as below:

$$F = \frac{(C_i / N_i)}{(C_o / N_o)}$$

It's easy to see that to reduce the noise factor, either the carrier signal has to go up, or the noise down. Resistors are a major contributor to noise, so eliminating or reducing them is crucial.

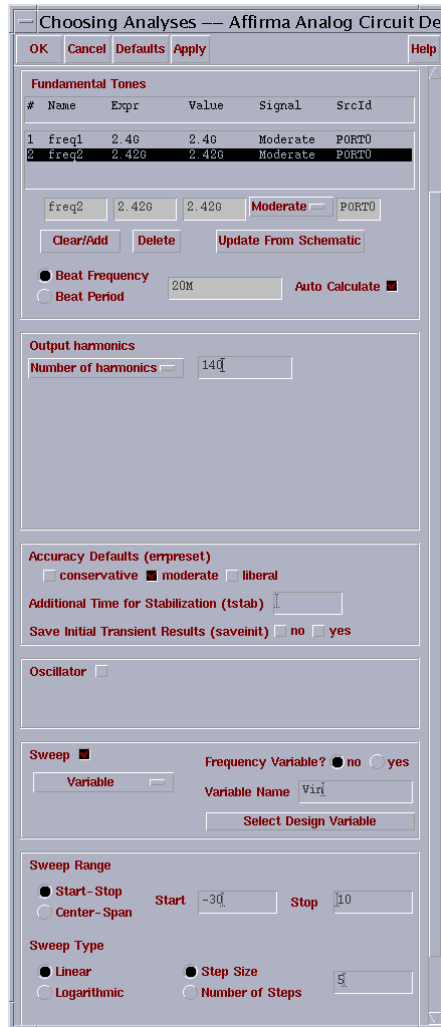


**Figure 7:** Noise Figure simulation results.

Cursor A marks the Noise Figure at the fundamental frequency (2.09 dB) and cursor B marks the minimum (2.044 dB). This noise figure is too high, it is above the spec. of 1.8dB. The ways to reduce this include making the amplifier device smaller, and/or splitting up the device into more fingers to reduce the series gate resistance.

### 1 dB Compression Point

Compression point and IP3 were simulated using the following simulator setups:



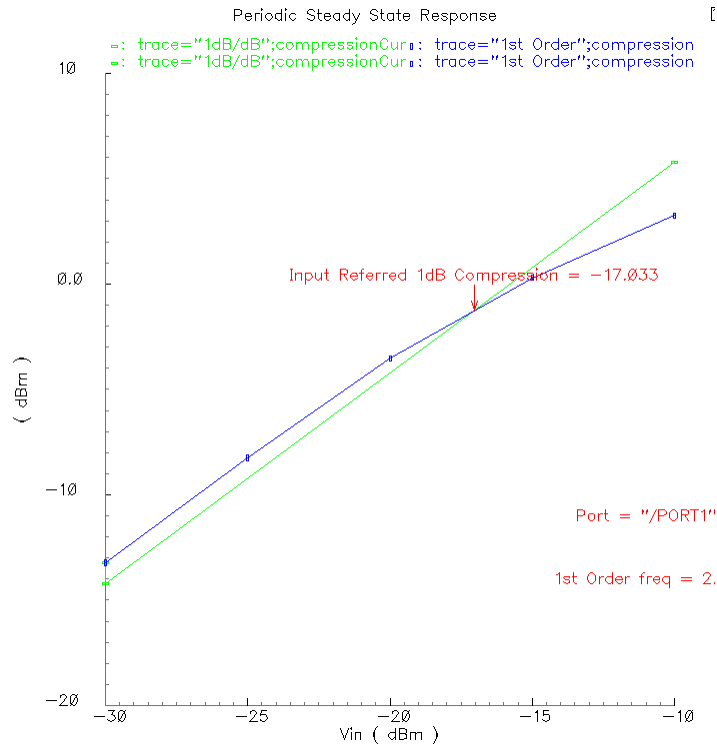
**Figure 8:** ssp simulation configuration.

The 1dB compression point is a measure of how much input power an amplifier can take before the output power is no longer proportional to the gain times the input by a factor of 1dB. In other words, as you keep increasing the input power, the gain will drop off. In our design, this happens at an input power of negative 17dBm.

A note on dBm: dBm is a measure of power relative to 1mW. The following expression is used to convert from one to the other:

$$P(\text{dBm}) = 10 \cdot \log(P(\text{mW})/1\text{mW})$$

Powers smaller than 1mW will result in negative dBm's. As an example, a power of 100mW will result in 20dBm.



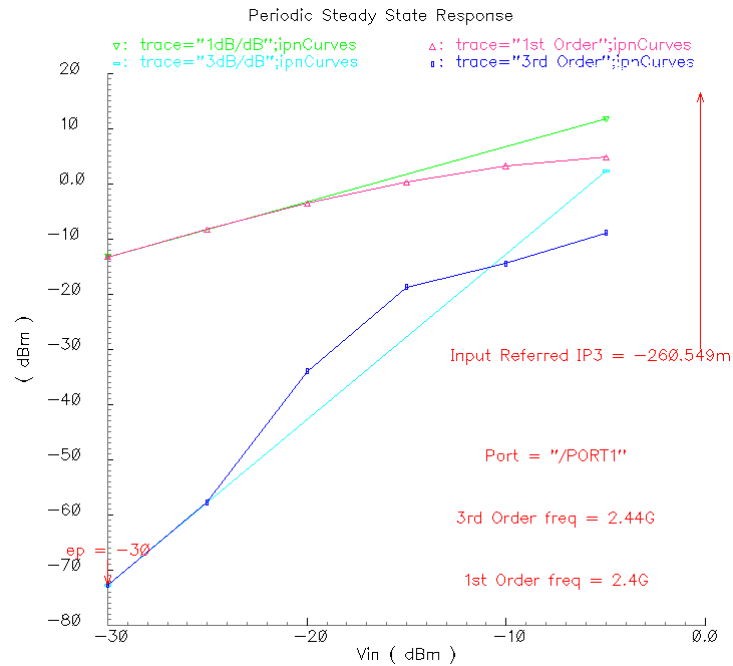
**Figure 9: 1 dB compression.**

If the input power  $V_{in}$  is increased beyond  $-10\text{dBm}$ , then the 1<sup>st</sup> order response (gain) will eventually settle to some saturation value.

### Third Order Intercept

Third order intercept (IP3) is a figure of merit for amplifiers (or mixers) which pinpoints the point at which the harmonic's power at the output is equal to the fundamental's power. When two frequencies are introduced into a non-linear system, harmonics will result. If these two frequencies are near each other then the harmonic will also be near the fundamental (input frequencies and their harmonics are evenly spaced). When the LNA is not tuned sharply enough, these harmonics can appear at the output with relatively large power.

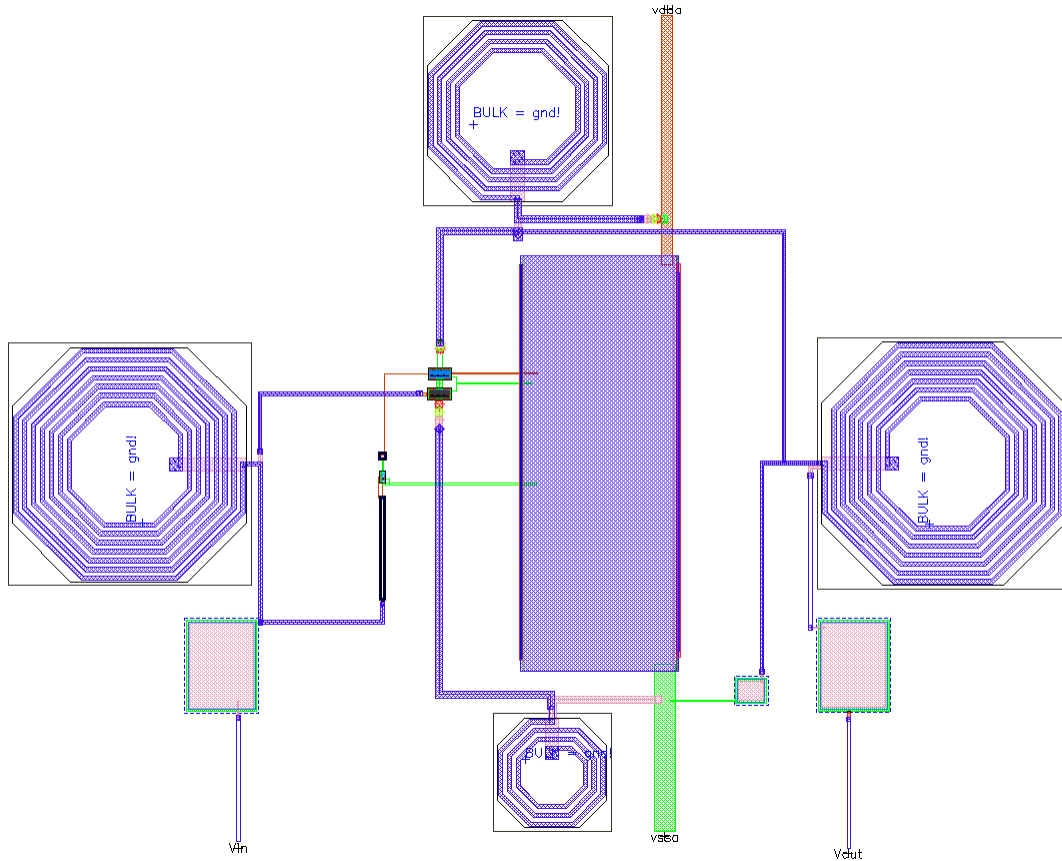
The following are the simulation results:



**Figure 10: IP3 simulation results.**

This simulation was not run long enough to actually see the lines intersect (green and teal), but the ideal lines continue in the same direction, so they do not need to be simulated out any further to get the intercept point. The ideal lines are derived from the simulation results (red and blue lines). The red line is the same as the curve we used to calculate the 1dB compression point and the blue curve is the harmonic signal content. Simulating further out in terms of input signal strength causes the circuit to enter breakdown and this severely slows down the simulation and can cause erroneous results.

## Layout



**Figure 11:** Layout full view.

In placing the devices, I considered the inductors to be the most important. In order to eliminate any coupling between inductors (hence, turning them into transformers), I placed these structures at least as far apart as they are wide. The basic device placement follows the device placement in the schematic. All interconnect routing (except routes to power and ground) were done using the topmost metal layer (AM) to minimize parasitic capacitance to ground. The circuit input is applied to the wire in the lower left and it can be seen that this is connected straight to the input coupling capacitor (MIM type). On the other side of the capacitor we can see the AC current blocking resistor which is connected to the bias transistor. The diode connected bias device is then connected to power through a bias resistor. The bias resistor was chosen to be the NWELL type because its tolerance is much tighter than the other resistor types and this will result in a much more accurate bias current. The AC blocking resistor is a poly type because it has a much smaller parasitic capacitance to ground.

The next devices are the gate inductor (on the left), the source inductor (bottom) and the amplifier transistors (near the middle) which are connected to the inductors. On the right we can see the impedance matching passives, and the output decoupling cap which is the larger of the two capacitors.

Power (vdda) is supplied from the top and ground (vssa) is connected at the bottom. The large structure in the center is essentially a very large MIM capacitor which functions as a coupling capacitor between power and ground. Extra wide wires (8um of AM layer) were used for high current carrying nets and plenty of vias were used when switching between metal layers.

The following is the DRC report:

```
icfb - Log: /home/ilk8123/CDS.log.2887
File Tools Options Technology File AMS utils Help 1
Inclusion limit is set to 1000.
Running drclayout analysis
Flat mode
Full checking.
DRC started.....Tue May 18 00:39:21 2004
completed...Tue May 18 00:41:12 2004
CPU TIME = 00:00:15 TOTAL TIME = 00:01:51
***** Summary of rule violation for cell "LNA_sim layout2" *****
# errors Violated Rules
1 #INFO: CMRF6SF DIVA DECK (REV DATE 12/12/2002) ####
1 GR844b: (M2 touching Q2) touching V1 found!
4044 GR611: V2 not within M3 found!
1 WARNING: GridCheck NOT RUN!
1 #INFO: 6 Level Metal (M1+M2+M3+M4+MT+AM/ML) PADS= WIREBOND #
4048 Total errors found
t
1 GR844b: (M2 touching Q2) touching V1 found!
mouse L: DJSelectObject() M: DJHiSetRefPoint() R: DJcycleSelSet()
>
```

**Figure 12:** DRC results.

Connectivity using LVS was not checked, however, flight lines were used during layout using the connectivity tool is Layout XL. This in no way guarantees connectivity, but it goes a long way.

## References:

1. M. Benmansour and P.R. Mukund, "A Tuned Wideband LNA in 0.25um IBM Process for RF Communication Applications," Dept. of Electrical Engineering, Rochester Institute of Technology.