Liquid Crystal Display (LCD) Technology

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I. Introduction

Liquid Crystal Displays (LCDs) are a display technology with many great features. Low power and an extremely small form factor make them an ideal display for portable devices. This paper will discuss the operating characteristics of liquid crystal technology and the architectures of LCDs. The LCD technology discussed in this paper pertains to the architectures most commonly found in portable electronic devices. Portable electronic devices pose a challenge because they require displays that are small in size, increase in resolution but also to remain as low power as possible.

II. Liquid Crystal Material Properties

Liquid Crystals (LC's) are molecules which under the influence of an electric field, align according to the field polarity. Liquid crystals are a type of dielectric and local regions polarize in an electric field as shown below in Figure 1 and Figure 2. The birefringence of the LC material is independent of the polarity of the voltage applied, therefore the birefringence depends on the RMS value of the voltage applied. Birefringence is the property that enables LC's to twist light as it passes through them. Polarizers are placed above and below the LC. Light is passed through the polarizers and the LC. The polarizers are arranged such that they are at a 90 degree angle to each other. When the LC is unengergized, it rotates the light passing through it such that it's direction matches that of the top polarizer. This lets all the light through. When a DC voltage is applied, light is unaffected while it passes though and the two polarizers block all light. The following diagram explains this driving method:

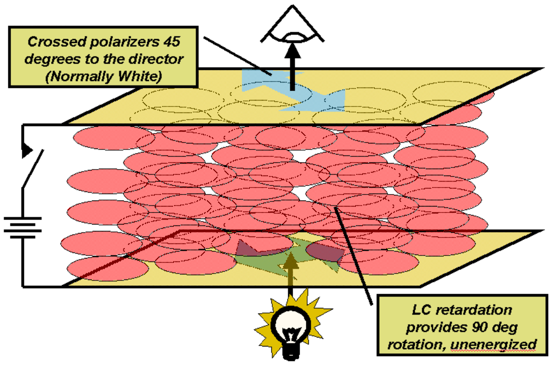

Figure 1: No Electric Field [1].

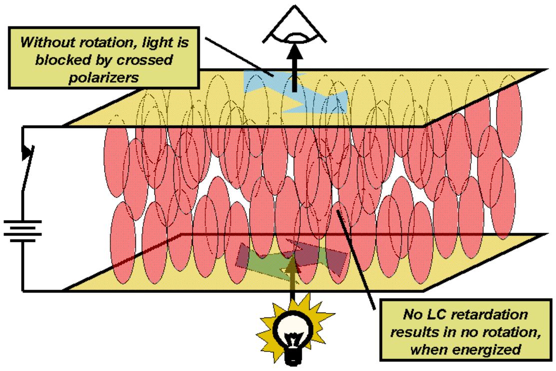

Figure 2: Electric field applied [1].

When driving an LCD, DC voltages are not used. Holding a DC value on a liquid crystal can cause electroplating of ion impurities on the electrodes. This electroplating is the major cause of image retention. To avoid this condition we need drive the LC with negative and positive voltages and make sure the average voltage on a liquid crystal is equal to zero. It's the RMS value of the voltage applied that will determine transmissivity. Below is a graph of an LCD's transmissivity versus the applied voltage:

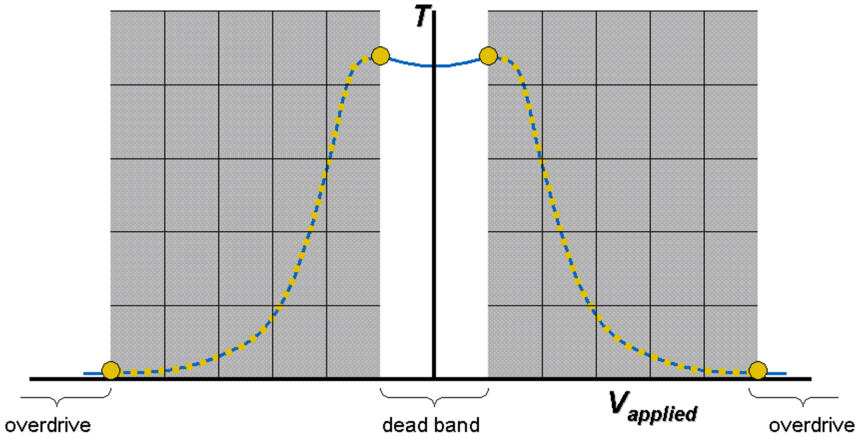

Figure 3: LC transmissivity versus voltage [1].

It can be seen from this figure that the LC's response to voltage is very non-linear. We can also see that this LC material has the same transmissivity whether the voltage applied to it is positive or negative, this is not always the case. Assuming we would like linear steps in transmissivity, we can see that some steps in transmissivity near the center of the range require small steps in voltage while the steps in transmissivity near the ends require larger steps in voltage. A digital to analog converter which is designed to drive an LC must be able to resolve the small voltage steps required near the center of the transmissivity curve. The slope of the tangent near this area will determine the resolution required by the converter.

III. Liquid Crystal Displays

This section will discuss the various types of Liquid Crystal Displays (LCDs). To create an amorphous silicon display, liquid crystal cells are arranged in a matrix to create a image. Pixels are arranged in columns and rows. A pixel contains three cells (also called subpixels), one to display each of the three primary colors - red, green and blue. To illuminate a display, white light (usually using a white LED) is shown through the display. Cells can output different colors because a red, green or blue film is deposited onto each cell in a pixel to filter the white light. Active matrix LCDs have transistors integrated on the glass to perform the row select.

Below is a simplified system diagram:

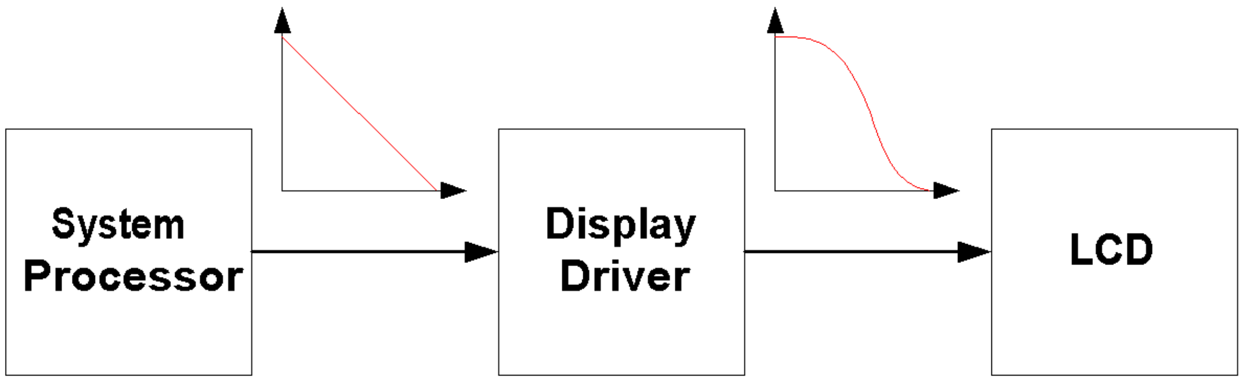

Figure 4: Simplified system diagram.

The system processor sends video commands or image data to the display driver and the display driver drives the analog voltages onto the LCD which will create the images. The system processor expects a linear relationship between the video data and the brightness on the display, therefore the display driver must create a nonlinear digital to analog conversion to obtain the linear response that is required. A typical LC material can only resolve approximately 64 steps in brightness, therefore 6 bits are used for each color for a total of 18 bits. There are two ways to perform the digital to analog conversion (DAC). The first is to use a nonlinear DAC with 6 bits of resolution which mimics the inverse of the response curve. The second is to use a high resolution DAC (approximately 8 to 10 bits) and a look up table (LUT) to create the inverse response curve. To determine the resolution needed for a linear DAC, we need to examine the transmissivity of the LCD. Below is a sample transmissivity curve:

Code	V	V Step (mV)
0	0.200	
1	0.218	18.1
2	0.236	18.1
3	0.254	18.1
4	0.272	18.1
5	0.292	20.1
6	0.318	25.2
7	0.348	30.3
8	0.383	35.2
9	0.423	39.9
10	0.467	44.2
11	0.515	47.5
12	0.566	51.0
13	0.621	55.8
14	0.683	61.7
15	0.750	66.6
16	0.821	71.4
17	0.897	76.1
18	0.978	80.7
19	1.064	86.3
20	1.152	87.9
21	1.236	84.0
22	1.321	84.6
23	1.407	86.4
24	1.496	89.0
25	1.589	93.0
26	1.686	97.2
27	1.780	93.4
28	1.862	82.5
29	1.939	76.1
30	2.011	72.8
31	2.082	70.4
32	2.154	72.3
33	2.220	66.3
34	2.285	64.3
35	2.347	62.8
36	2.409	62.0
37	2.463	53.8
38	2.517	53.5
39	2.567	50.6
40	2.618	51.1
41	2.671	53.0
42	2.722	50.4
43	2.771	49.0
44	2.815	44.4
45	2.861	45.9
46	2.908	47.1
47	2.957	48.4
48	3.003	46.9
49	3.047	43.3
50	3.096	48.8
51	3.146	50.8
52	3.198	51.7
53	3.251	52.4
54	3.303	52.7
55	3.367	63.4
56	3.426	59.4
57	3.494	68.5
58	3.568	73.4
59	3.647	79.5
60	3.741	93.6
61	3.866	124.8
62	4.035	169.8
63	4.800	764.5

Min V Step:	18.1

Figure 5: Sample Transmissivity curve.

We can see that the minimum step is 18.1mV. This corresponds to 277 steps over the entire 5V range. 277 steps implies that a 9-bit converter is necessary.

A. Amorphous Silicon Active Matrix Displays (AMLCD)

Amorphous Silicon (or Active Matrix) LCD displays are currently the most common because large sheets of it are easily and cheaply manufactured. Silicon is deposited on the glass, but it ends up only in an amorphous state because the glass cannot stand the temperatures required for annealing. These transistors are too slow to form logic and other complex circuits because their charge carrier mobility is so low. Fortunately, transistors good enough to switch a pixel in and out can still be created. Below is a diagram of a portion of an LCD:

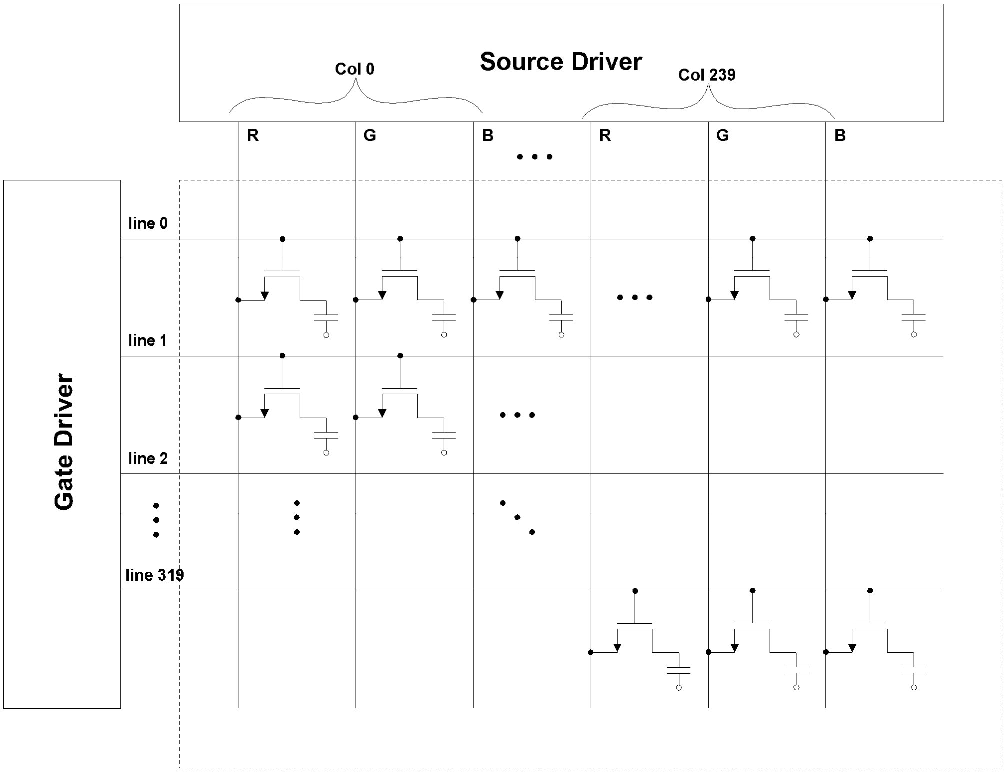

Figure 6: Amorphous Silicon LCD architecture.

As shown in Figure 5, LCD displays require many connections to the row and column drivers,. The most common display driver configuration attaches the silicon driver circuits directly to the glass using a “flip-chip” technique. Both the source driver and gate driver are connected directly to the glass and the required components and system controller are connected to the glass using a flexible circuit board.

It can be seen that that the gate driver selects an entire row of pixels at a time. The gate driver steps through all the lines in succession down through the whole display (Figure 6). The LC cell is represented by the capacitor attached to the pass transistor. When a pixel (one site across the line) is selected, it’s transistor connects the LC site to it's associated column line. Then the source driver applies the appropriate voltage onto the pixel. The other terminal of the LC cells (basically a capacitor) are all connected to a common backplane. To avoid electroplating as mentioned in Section II, we need to apply a driver voltage signal to the LC where the time average value for successive write patterns is zero volts (no dc content). This is done by raising the common plate voltage to somewhere around 5V and then applying a voltage range of 0 – 5V on the columns.

Amorphous silicon displays typically require higher drive voltages than provided by standard CMOS integrated circuit processes. The gates need to be driven to +10V to turn the transistors on and they need to be driven to –5V to turn them fully off. Connection configurations become more complex as the display resolution increases. A quarter VGA display (320x240) would require 960 connections by the source driver IC and 320 connections by the gate driver IC. This connection arrangement is unfeasible due to pad number limitations and the space on the LCD required to route drive signals.

B. Low Temperature Polysilicon Displays (LTPS)

In LTPS displays, the thin layer of amorphous silicon is heated up to create polysilicon. This is done by using an excimer laser to locally heat up the silicon thus keeping the display temperature under the 450^{O}C glass limit. The annealed silicon has a charge carrier mobility which can reach up to 90% of the mobility of traditional silicon [2]. In addition, the annealing process enables CMOS devices to be fabricated directly on the glass. This technology allows for a wide array circuits to be integrated on the display surface, including most of the gate driver. Therefore, only one external chip is required to drive the LTPS LCD. Figure 7 shows a typical LTPS architecture.

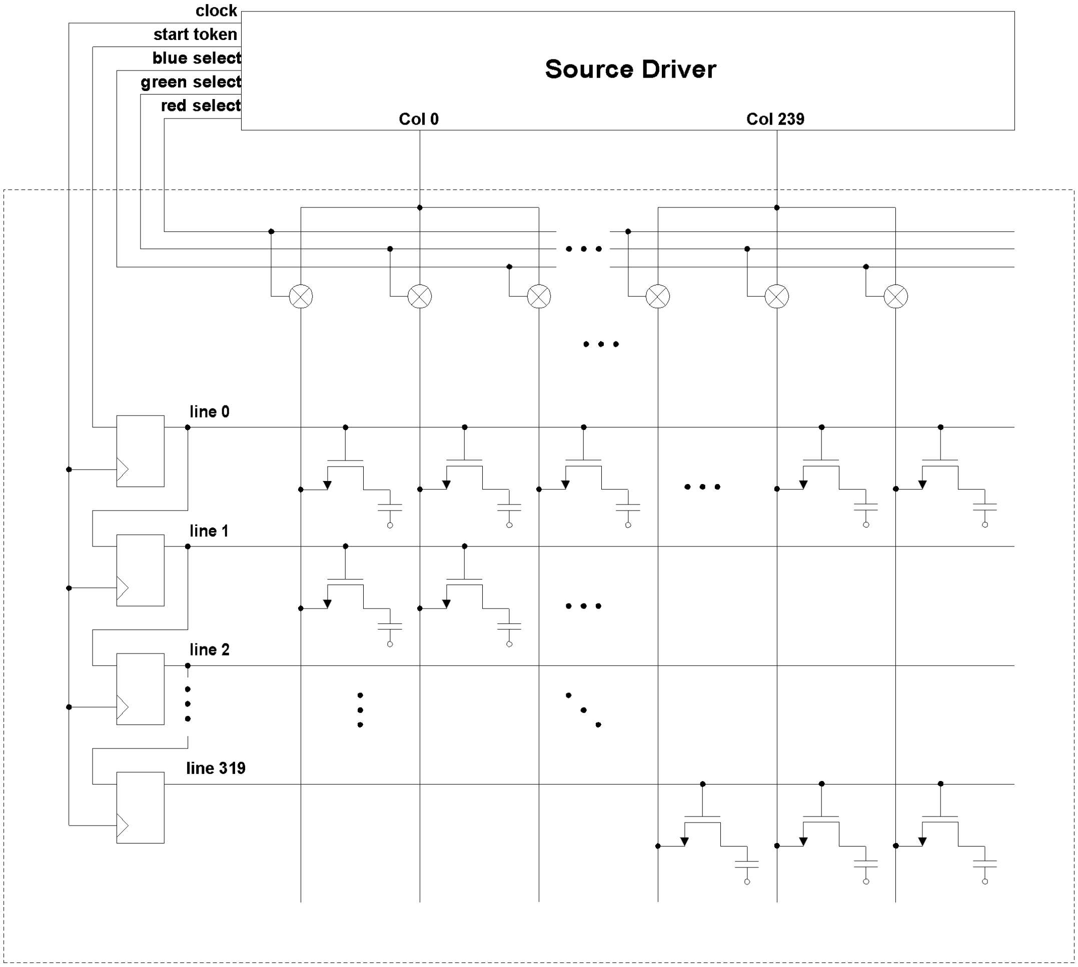

Figure 7: Typical LTPS LCD architecture.

In this LTPS architecture, the gate driver is integrated onto the glass. Here the gate driver is a simple register chain which passes a token down through the chain at the clock rate. This will select one line and turn the rest off. This architecture has just saved one entire piece of silicon – the gate driver. Another benefit of LTPS LCD displays is the reduced voltage requirements to drive the LCD. This makes it possible to use a cheaper more advanced process. The last difference is a three to one multiplexer for every column. This reduces the number of connections to the glass required by the source driver to one third of what is required by the amorphous LCD displays. Unfortunately this also requires the column driver to be three times as fast because three groups of sub-pixels must be driven during every line.

C. Continuous Grain Silicon (CGS)

Continuous Grain Silicon promises an even higher level of integration. This process, pioneered by Sharp, allows the creation of transistors which are about 600 times faster than amorphous based devices and approximately three times faster than LTPS [3]. CGS allows an even higher level of multiplexing which allows even fewer connections to the LCD due to better transistors and reduced parasitics on the glass. The use of better transistors allows the LCD makers to create smaller and higher resolution displays. Figure 7 is a system diagram showing a typical CGS display.

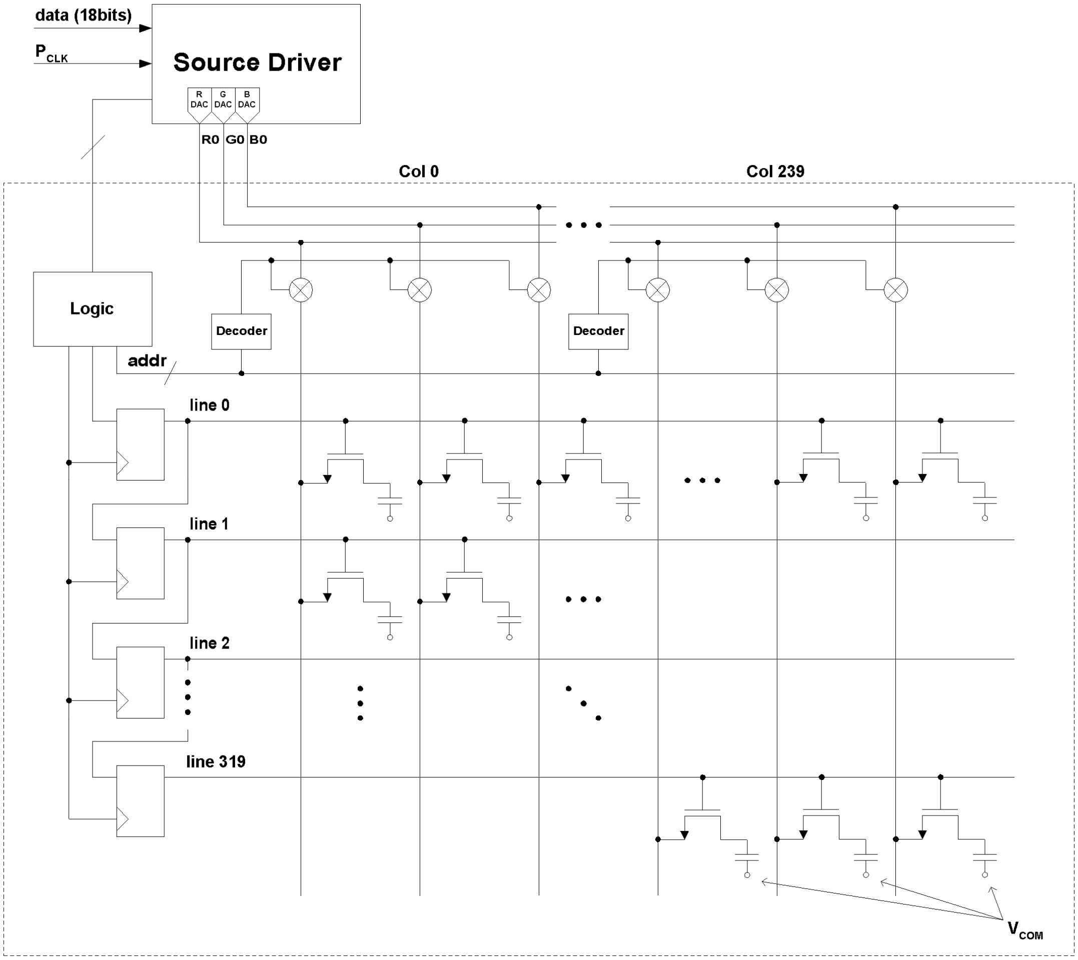

Figure 8: CGS LCD architecture.

In the CGS LCD architecture, the connections to the glass have been reduced to perhaps a few dozen. Signal that are needed include the power supply, control signals for the gate driver/multiplexer function and the analog outputs. One advantage of this architecture is that it is now possible to attach the source driver to the LCD using a flexible circuit board. By avoiding mounting the chip on the glass, glass area can be saved resulting in more LCDs per sheet. In the diagram above it is shown that only one set of RGB is connected to the glass to simplify the figure. In actual CGS displays, there are usually three or more sets of RGB lines multiplexed on the glass to decrease the speed requirements of the Digital to Analog converter in the source driver. In the following example we will assume there is one set of RGB lines to keep it simple. In this example, a checker board pattern will be used on the display. This keeps R, G and B the same voltage, but voltages will be continuously toggling both in the horizontal and vertical directions. The checkerboard pattern is below:

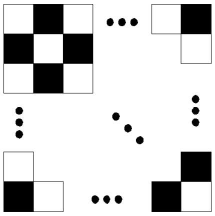

Figure 9: Checkerboard LCD pattern.

The example will also employ line inversion to keep the DC voltage on the pixels equal to zero. This means positive voltages will be driven onto the pixels on one line (VCOM is low) and then negative voltages are driven onto the display one the next line when VCOM is high. The glass type is normally black which means that the LCD does not let light through when the LC is unenergized. The following is a sample diagram showing operation of a generic CGS LCD with the checkerboard pattern:

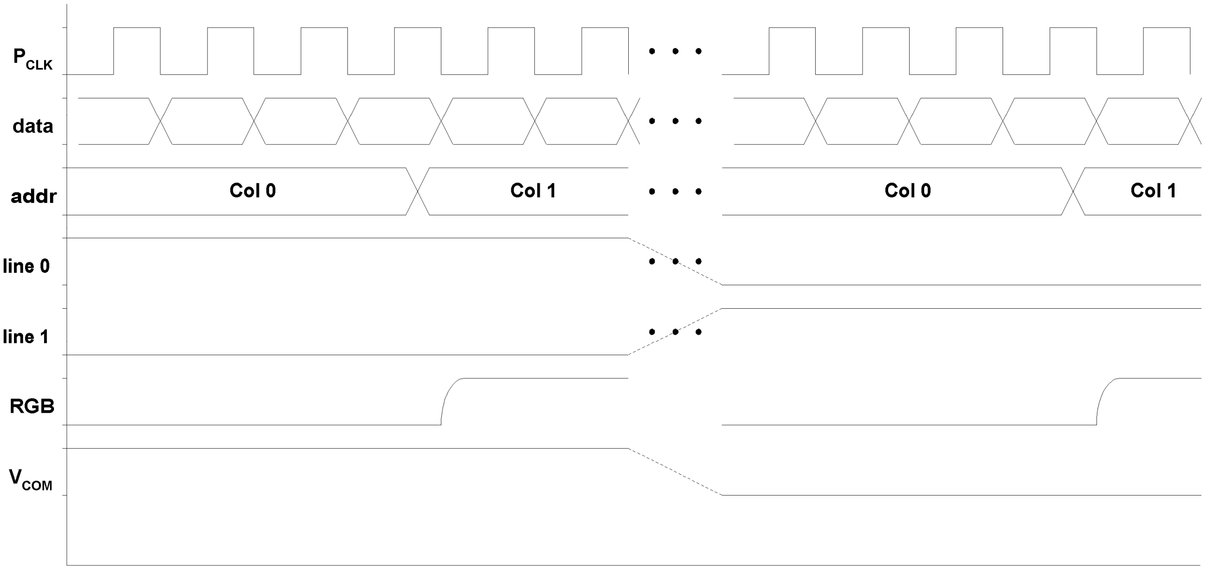

Figure 10: CGS timing diagram.

Note in the above diagram that there is a negative voltage on the first white pixel on the first line and there is a positive voltage on the second pixel (also white) on the second line. Both pixels display white, but the second's voltage is the opposite of the first pixel's voltage.

The following equations show just how fast the DAC needs to be to drive a modern CGS display. We will assume the CGS display has four sets of RGB lines multiplexed on the glass, with a display size of 320 by 240 (quarter VGA), and a refresh rate of 60 frames per second. We calculate the line rate and conversion time to estimate the expected performance of the DAC source drivers.

$$line\_rate = \frac{1}{f_{rate} \times N_{lines}} = \frac{1}{60 \cdot 320} = 52\mu s$$

where f_{rate} is the frame rate (update rate) and N_{lines} is the number of lines in the display. In our display, we are driving 4 pixels at a time out of 240 total pixels per line. This results in:

$$pixel\_time = \frac{T_{line}}{N_{mux}} = \frac{52\mu s}{60} = 870ns$$

where T_{line} is the line time and N_{mux} is the multiplexing factor. The multiplexing factor is simply the number of column lines divided by the number of RGB lines driven by the source driver, in the case of the above example, it is four.

If we consider the parasitics along the column line and the subpixel switch resistance, there is some additional settling time required before we can switch to the next column to make sure the LC voltage has settled. Below is a simplified RC load which describes the panel parasitics.

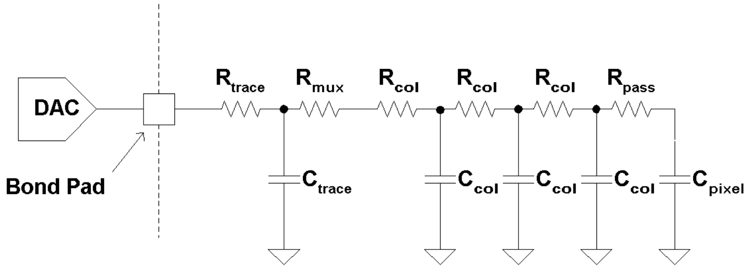

Figure 11: Panel parasitic along signal path.

The dotted line signifies the partition of the chip and the LCD. The column line resistance and capacitance is the major contributor to delay. Here it is broken down into a three RC network to better simulate the actual load which looks much like a transmission line.

Because of these parasitics, there is a trade off between the number of RGB's multiplexed on the glass and the source driver's power. There is also an intrinsic limitation due to panel settling time. For example, the settling time to charge the pixel furthest away from the source driver might take 200ns, therefore, only having one set of RGB's on the glass is impractical due to the fact that the source driver's outputs would have almost no time at all to settle. This is the reason a typical CGS LCD will have four sets of RGB lines for a total of 12 analog drivers.

Due to the RC delay, approximately half of the *pixel_time* should be used as the settling time requirement for the DAC. This results in a settling time of 400ns which corresponds to a conversion rate of 2.5MHz.

D. Small Format Versus Large Format

This paper focuses on small format displays, but it is worth the space to mention some differences. The biggest and most important difference is size. This causes the column line capacitances to be vastly larger. In addition there are many more columns to drive, so it is no longer possible to drive the entire panel with one IC. Small format drivers have a centralized buffer (voltage generator) scheme, whereas a large format LCD driver has a buffer per channel because of the large capacitance. To save power and space, small format drivers minimize the number of buffers because it is possible to drive many columns at a time by one buffer.

References

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3. Sharp Microelectronics Announces Continuous Grain Silicon Display, Sharp Microelectronics, http://www.sharpsma.com/sma/pressroom/press.htm?newsid=22